SPECIFICATION

AGO-101S0-NN-N

Atualizado pelo MKT em 15/02/2016

Record of Revision

Version	Revise Date	Page	Content
Pre-spec.A	2015/06/16		Initial Release

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	10.1 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	1024 × 3(RGB) ×600	
4	Display mode	Normally White, Transmissive	
5	Pixel pitch	0.2175(H) X 0.2088(V) X RGB mm	
6	Active area	222.72(H) X 125.28(V) mm	
7	Outline dimensions	235(H) X 143(V) X 5.0(D) mm	
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	TTL-24BIT	
11	Backlight Power consumption	TBD	
12	Panel Power consumption	TBD	
13	Weight	TBD	

2. Pin Assignment

FPC Connector is used for the module electronics interface. The recommended model is FH12A-50S-0.5SH manufactured by Hirose.

Pin No.	Symbol	I/O	Function	Remark
1	LED+	P	Power for LED backlight(anode)	
2	LED+	P	Power for LED backlight(anode)	
3	LED-	P	Power for LED backlight(Cathode)	
4	LED-	P	Power for LED backlight(Cathode)	
5	GND	P	Power ground	
6	V_{COM}	I	Common voltage	
7	DVDD	P	Power for Digital Circuit	
8	MODE	I	DE/SYNC mode select	Note 1
9	DE	I	Data Input Enable	
10	VS	I	Vertical Sync Input	
11	HS	I	Horizontal Sync Input	
12	B7	I	Blue data(MSB)	
13	B6	I	Blue data	
14	B5	I	Blue data	
15	B4	I	Blue data	
16	B3	I	Blue data	
17	B2	I	Blue data	
18	B1	I	Blue data	Note 2
19	B0	I	Blue data(LSB)	Note 2
20	G7	I	Green data(MSB)	
21	G6	I	Green data	
22	G5	I	Green data	
23	G4	I	Green data	
24	G3	I	Green data	
25	G2	I	Green data	
26	G1	I	Green data	Note 2

27	G0	I	Green data(LSB)	Note 2
28	R7	I	Red data(MSB)	
29	R6	I	Red data	
30	R5	I	Red data	
31	R4	I	Red data	
32	R3	I	Red data	
33	R2	I	Red data	
34	R1	I	Red data	Note 2
35	R0	I	Red data(LSB)	Note 2
36	GND	P	Power Ground	
37	DCLK	I	Sample clock	Note 3
38	GND	P	Power Ground	
39	L/R	I	Left / right selection	Note 4,5
40	U/D	I	Up/down selection	Note 4,5
41	V_{GH}	P	Gate ON Voltage	
42	V_{GL}	P	Gate OFF Voltage	
43	AV_{DD}	P	Power for Analog Circuit	
44	RESET	I	Global reset pin.	Note 6
45	NC	-	No connection	
46	V_{COM}	I	Common Voltage	
47	DITHB	I	Dithering function	Note 7
48	GND	P	Power Ground	
49	NC	-	No connection	
50	NC	-	No connection	

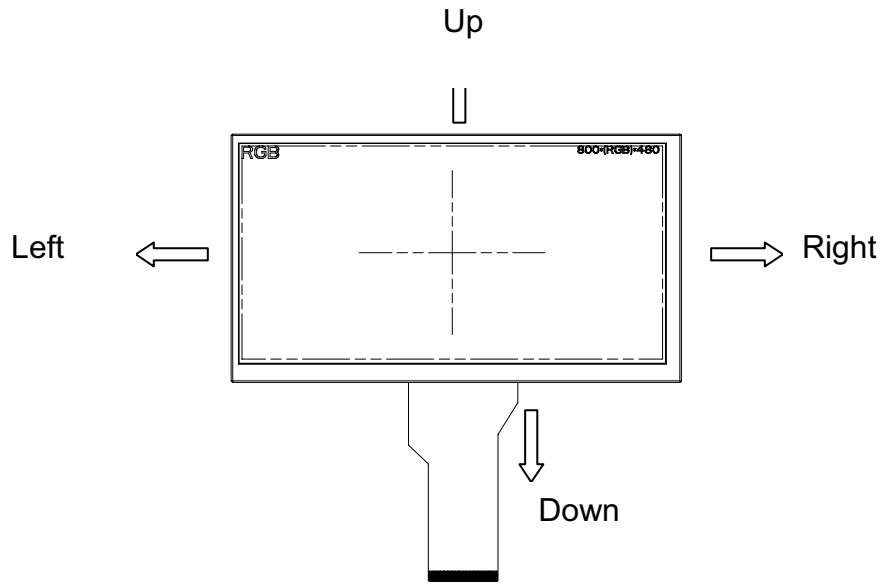
I: input, O: output, P: Power

Note 1: DE/SYNC mode select. Normally pull high.
When select DE mode, MODE=”1”, VS and HS must pull high.
When select SYNC mode, MODE= ”0”, DE must be grounded.
Note 2: When input 18 bits RGB data, the two low bits of R,G and B data must be grounded.
Note 3: Data shall be latched at the falling edge of DCLK.

Note 4: Selection of scanning mode

Setting of scan control input		Scanning direction
U/D	L/R	
GND	DV_{DD}	Up to down, left to right
DV_{DD}	GND	Down to up, right to left
GND	GND	Up to down, right to left
DV_{DD}	DV_{DD}	Down to up, left to right

Note 5: Definition of scanning direction.
Refer to the figure as below:



Note 6: Global reset pin. Active low to enter reset state. Suggest to connect with an RC reset circuit for stability. Normally pull high.

Note 7: Dithering function enable control, normally pull high.
When DITHB="1",Disable internal dithering function,
When DITHB="0",Enable internal dithering function,

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	DV_{DD}	-0.3	5.0	V	
	AV_{DD}	-0.5	15	V	
	V_{GH}	-0.3	40.0	V	
	V_{GL}	-20.0	0.3	V	
	V_{GH}-V_{GL}	-	40.0	V	
Operation Temperature	T_{OP}	-20	55	℃	
Storage Temperature	T_{ST}	-20	60	℃	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.1.1. Typical Operation Conditions

(Note 1)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV_{DD}	3.0	3.3	3.6	V	
	AV_{DD}	9.5	10.0	10.5	V	
	V_{GH}	14	15	16	V	
	V_{GL}	-10	-9	-8	V	
Input signal voltage	V_{COM}	3.8	4.0	4.2	V	

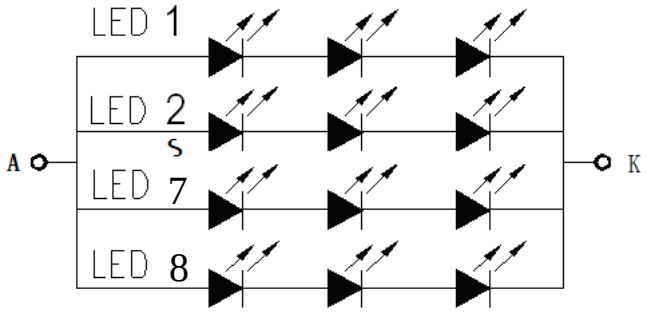
Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.
Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.

3.1.2. Current Consumption

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{GH}	-	0.5	5.5	mA	V_{GH} =15V
	I_{GL}	-	4.8	9.8	mA	V_{GL} =-9.0V
	IDV_{DD}	-	17.9	22.9	mA	V_{DD} =3.3V
	IAV_{DD}	-	29.1	34.1	mA	AV_{DD} =10.0V

3.1.3. Backlight Driving Conditions (24 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	8.7	9.6	10.5	V	Note 1
Current for LED backlight	IL	120	160	200	mA	
Luminance (on the module surface,BM-7)		100	150	-	cd/m^2	
LED life time	-	50,000	-	-	Hr	Note 2

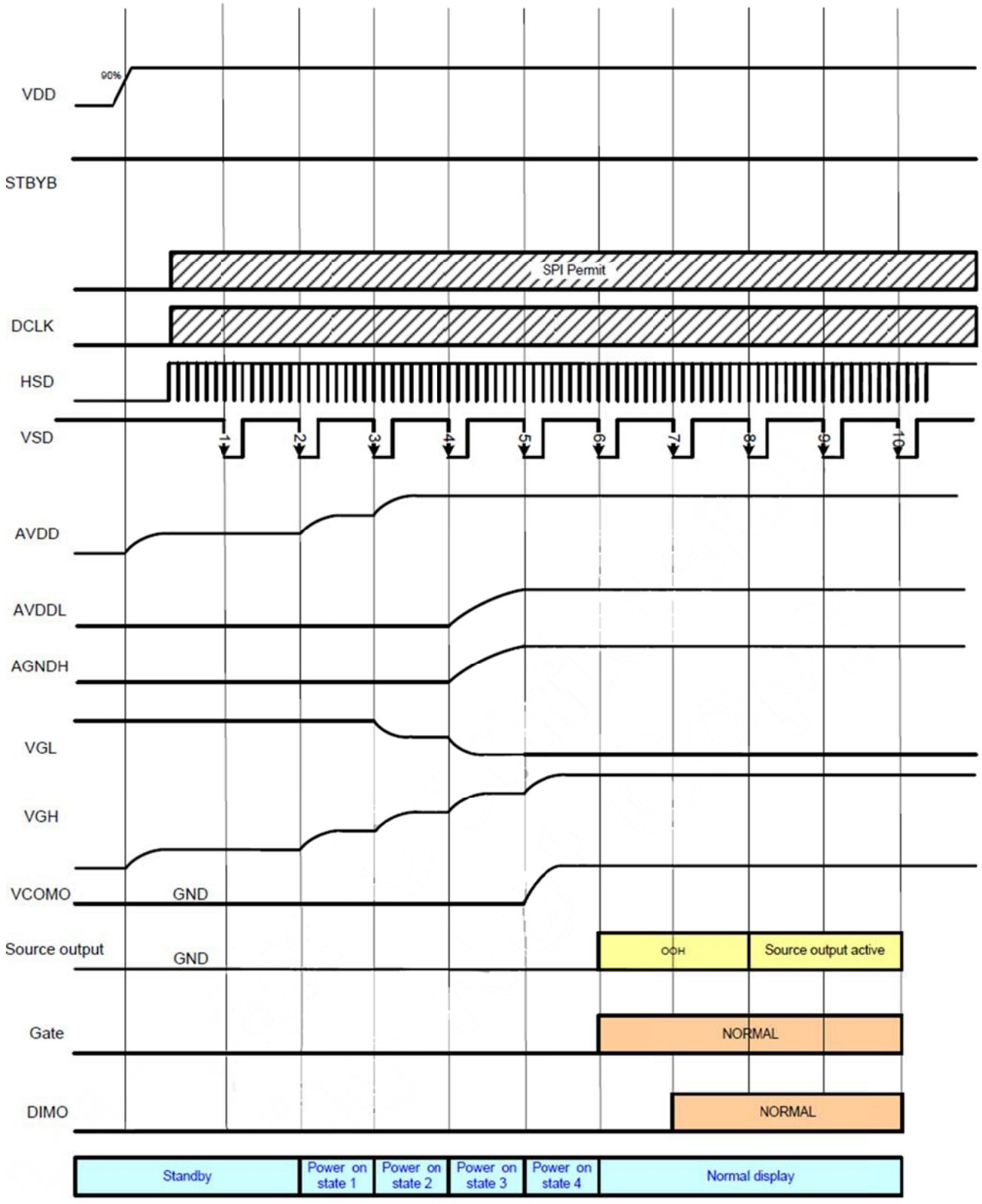


3.2. Power Sequence

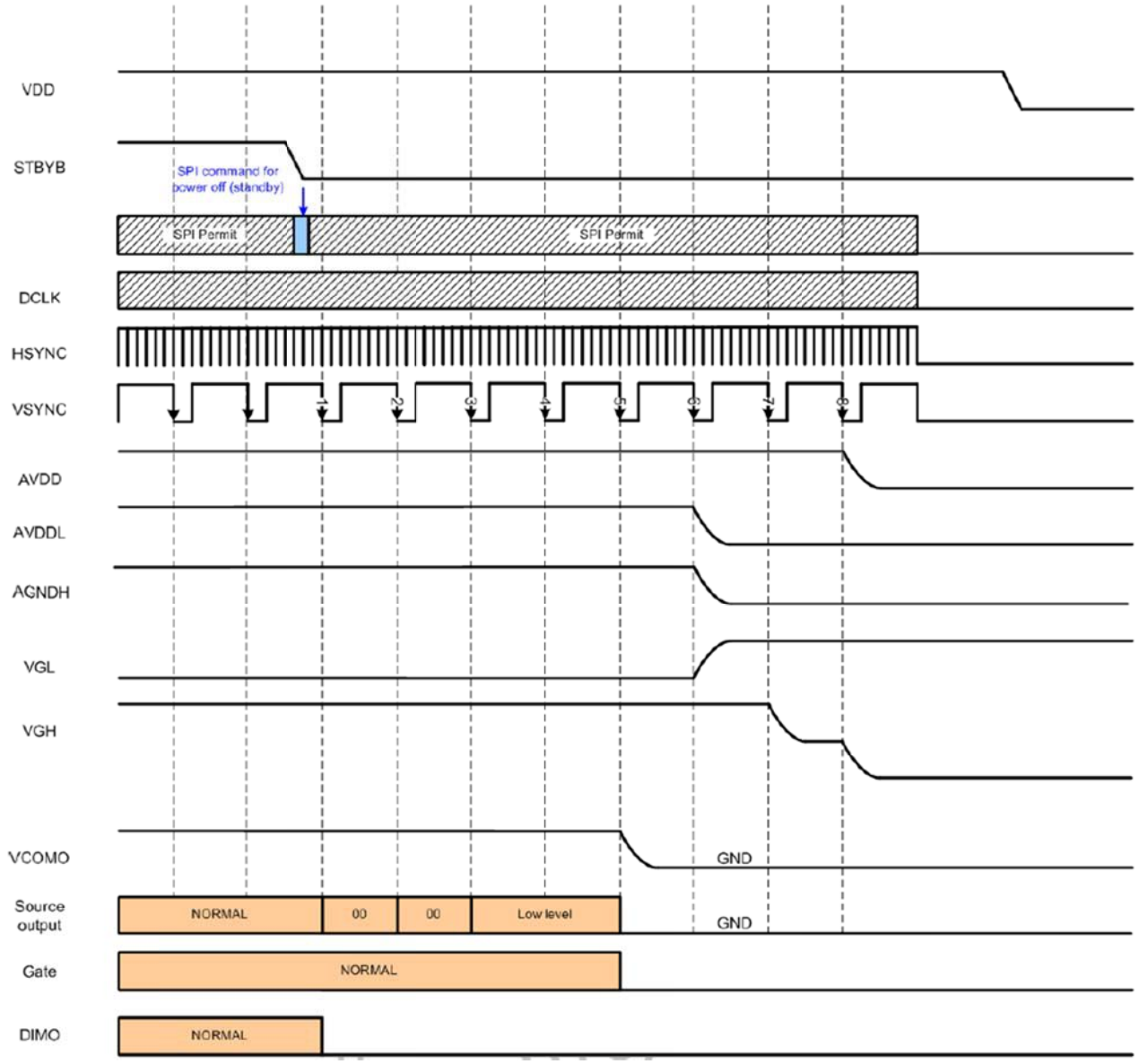
To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power on: VDD, GND → AVDD, AGND → V1 to V14

Power off: V1 to V14 → AVDD, AGND→ VDD, GND



Power on timing sequence



Power off timing sequence

Note: Low level=3FH, when NBW=L (Normally white)

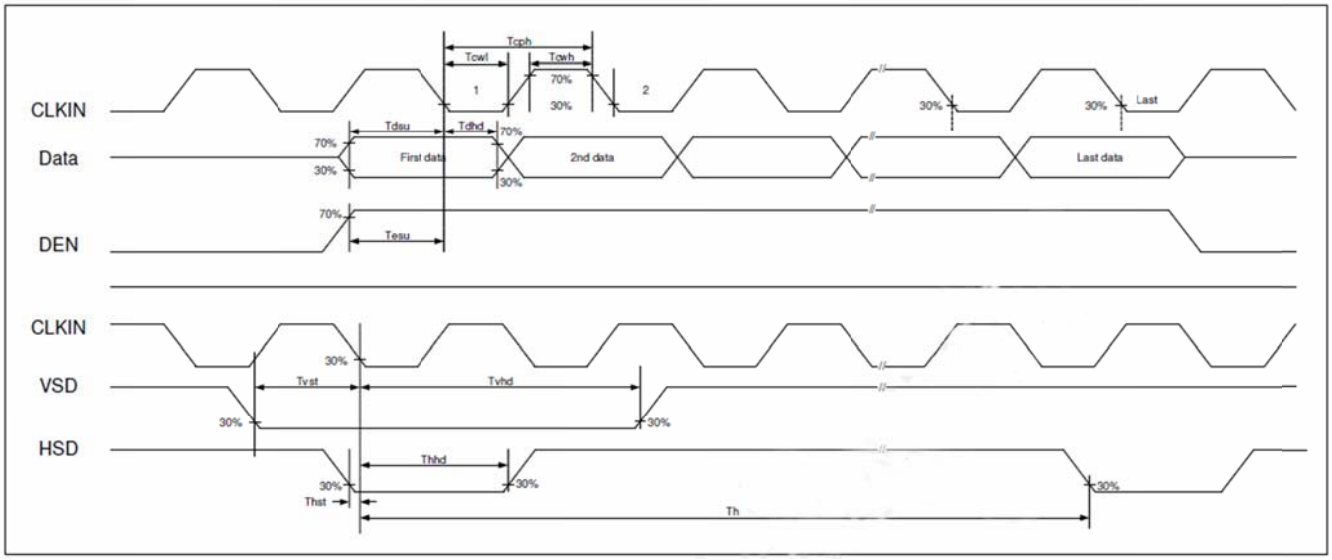
Low level=00H, when NBW=H (Normally black

3.3. Timing Characteristics

3.3.1. AC Electrical Characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
VDD Power On Slew rate	T_{POR}	-	-	20	ms	From 0V to 90% VDD
GRB pulse width	T_{Rst}	50	-	-	us	DCLK=65MHz
DCLK cycle time	T_{cph}	14	-	-	ns	
DCLK pulse duty	T_{cwh}	40	50	60	%	
VSD setup time	T_{vst}	5	-	-	ns	
VSD hold time	T_{vhd}	5	-	-	ns	
HSD setup time	T_{hst}	5	-	-	ns	
HSD hold time	T_{hhd}	5	-	-	ns	
Data set-up time	T_{dsu}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
Data hold time	T_{dhd}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
DE setup time	T_{esu}	5	-	-	ns	
DE hold time	T_{ehd}	5	-		ns	
Output stable time	T_{sst}	-	-	6	us	10% to 90% target voltage.CL=90pF, R=10K ohm(Cascade)
				3		Dual gate

3.3.2. Input Clock and Data Timing Diagram



3.3.3. Timing

DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd		600		TH
VSD Period	tv	610	635	800	TH
VSD Blanking	tvbp+ tvfp	10	35	200	TH

HV mode

Horizontal timing

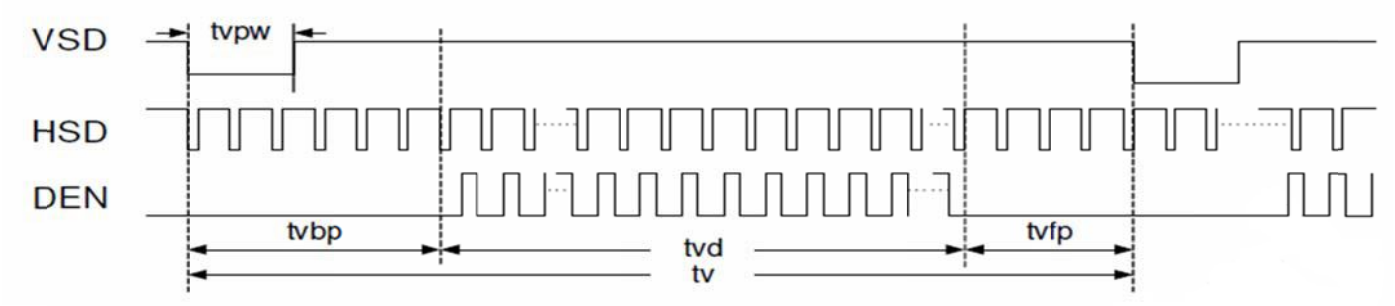
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	44.9	51.2	63	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp		160		DCLK
HSD Front Porch	thfp	16	160	216	DCLK

Vertical Timing

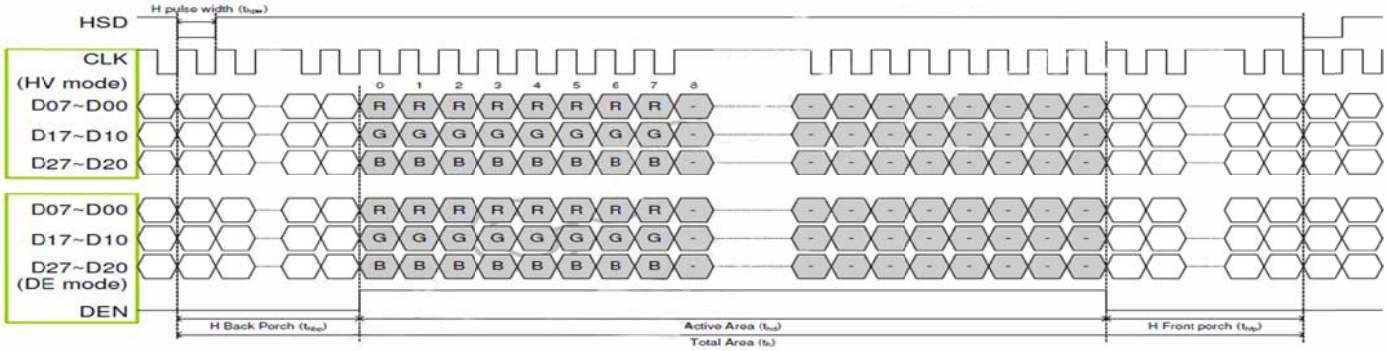
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		600		TH
VSD Period	tv	624	635	750	TH
VSD Pulse Width	tvpw	1	-	20	TH
VSD Back Porch	tvbp		23		TH
VSD Front Porch	tvfp	1	12	127	TH

3.3.4. Data Input Format

Vertical Timing



Horizontal Timing



4. Optical Specifications

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70	--	Degree	Note1
		θB		40	50	--		
		θL		60	70	--		
		θR		60	70	--		
Contrast Ratio		CR	θ=0°	500	600	--		Note4
Response Time		$T_{ON}+T_{OFF}$	25℃	--	8	--	ms	Note3
Chromaticity	White	x	Backlight is on	0.237	0.277	0.317		Note2 Note5 Note6
		y		0.266	0.306	0.346		
	Red	x		0.550	0.590	0.630		
		y		0.300	0.340	0.380		
	Green	x		0.301	0.341	0.381		
		y		0.554	0.594	0.634		
	Blue	x		0.117	0.157	0.197		
		y		0.075	0.115	0.155		
Uniformity		U		70	80	--	%	Note7
NTSC				--	50	--	%	
Luminance		L		100	150	--	cd/m^2	Note6

Test Conditions:

1. DV_{DD}=3.3V, I_L = 160mA(Backlight current),the ambient temperature is 25℃.
2. The test systems refer to Note 2.

5. Mechanical Drawing